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DIGITAL INTERMEDIATE FREQUENCY QAM MODULATOR USING PARALLEL PROCESSING

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This applications claims priority to U.S. Provisional Patent Application Serial No. 60/404596, titled "Digital IF Modulator Using Parallel Processing" filed August 19, 2002, incorporated herein by reference.

The United States Government has rights in this invention pursuant to Contract No. W-7405-ENG-48 between the United States Department of Energy and the University of California for the operation of Lawrence Livermore National Laboratory.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to digital quadrature amplitude modulation, and more specifically, it relates to a digital intermediate frequency (IF) modulator which can be implemented with low cost field programmable gate arrays (FPGAs) to generate very high IF carrier frequencies.

Description of Related Art

Figure 1A depicts a prior art digital Quadrature Amplitude Modulation (QAM) Intermediate Frequency (IF) modulator using a Numerical Control Oscillator (NCO) **1010** and multipliers **1000** and **1030**. QAM employs modulation where phase and amplitude are changed according to data input signals. The method is bandwidth efficient but requires high amplitude and phase accuracy. The data input signal is a complex signal that consists of real and imaginary parts. In digital communication, I (In-phase) and Q (Quadrature phase) are used to represent real and imaginary parts. There are M possible symbols, and thus, the technique is normally written as M-QAM. A symbol represents one point in the I/Q constellation. Symbol rate is bit rate divided by $\log_2 M$.

The **1070** module converts input data from bit rate to symbol rate that is determined by the type of digital M-QAM modulator selected. The serial data

are digital in strict sense, and are coming from any digital device at 1 bit per clock cycle. The grouping of the serial bits into k-bits follows the equality k =log2M, where M is the M-QAM modulation scheme. Each group of k-bits are then fed in parallel to the **1060**, where the k-bits are mapped into I-bits and Q-bits parallel data. The numbers of I-bits and Q-bits are mapped according to the selected M-QAM constellation. For a square constellation, the numbers of I-bits and Q-bits= k-bits/2. The value of the I-bits and Q-bits represented is determined by the type of mapping used. For instance, GRAY coding requires that I and Q have values that are different by no more than one logical position. **1080** and **1100** performs the pulse shaping on the I-bits and Q-bits of data to remove the intersymbol interference (ISI), as well as reducing the radio bandwidth. The **1090** and **1200** adds more zero data samples to the output of the **1080** and **1100** to match the speed of the **1012** and **1013** prior to digitally multiplying the digital samples at **1000** and **1030**. And the results are added digitally at a **1020** to produce the digital modulated carrier. The operation is done at DAC's speed, which is lots higher than the symbol rate, typically, the DAC's speed is more than 10 times that of the symbol rate. The **1020** digital data samples are converted to analog waveform via DAC. This is the Intermediate Frequency (IF) since it is sent further down the chain to the RFE (Radio Front End) for amplification, filtering, and final carrier upconversion prior to transmission.

Figure 1B is a prior art block diagram illustrating how the sine IF frequency is generated by the NCO. The sine carrier frequency, of Phase accumulator **1011** is generated by successively adding the phase M-word loaded into the parallel phase register until the phase accumulator is overflowed, which is then addressed to the sine ROM **1013**. The digital sine and cosine output is then sequentially multiplied to the digitally filtered I and Q after band-limiting and interpolation to the matched fc, which is the sampling frequency of the Digital to Analog converter (D/A).

Referring again to Figure 1A, the digital output of the NCO at **1020** is $S(n) = Ai(n)Cos(\omega_{if}t(n)) + Aq(n)Sin(\omega_{if}t(n))$, where ω_{if} is the output frequency of the NCO and Ai(n) and Aq(n) are the quadrature data symbols.

A drawback from the use of an NCO is that the Digital IF QAM Modulator requires two multipliers **1000** and **1030**, which results in inefficient field programmable gate array (FPGA) implementation. FPGA is a generic terminology for programmable logic device, all digital design are realizable using FPGA, or ASIC.

Additionally, **1012** and **1013** require large ROMs in order to achieve acceptable spectral purity. The size of ROM is $(2^k \times M)$, where k is the truncated phase address, which is normally 14 bits or above, and M is the bus width of the ROM (typically determined by the DAC resolution, e.g., 8-bit to 12-bits, without compression). Furthermore, the sequential operation of the NCO, multiplier,

and adder logic demands that the digital operation speed be the same as that of fc (sampling frequency). As a result, for higher fo frequency, an increase in power and cost will result. fo is an output frequency generated after the digital data are fed through the DAC (digital to Analog Converter). The Nyquist requirement dictates that the fc greater or equal to 2fo frequency.

Figure 2 depicts a Coordinate Rotation Digital Computer (CORDIC)-based digital QAM modulator. CORDIC **1100** implements the same functions as the cosine and sine ROMs of Figure 1A, using arrays of adders and subtractors. The goal is to remove the multipliers and sine/cosine ROMs, which cannot be realized efficiently using FPGAs or Application Specific Integrated Circuits (ASICs). According to WO 00/65799, the CORDIC circular rotator performs small successive rotations to achieve the phase to amplitude conversion without the use of Sine and Cosine ROMs.

A drawback of the CORDIC-based digital QAM IF is that its modulator phase accumulator operates at the same speeds as the D/A, and thus demands more power, which translates directly to high cost and more spectrum noise. For upsampling, the D/A sampling speed is at least 3 times the phase accumulator speed. For an 80 MHz IF modulator carrier, this requires a FPGA normal operating speed of 240 MHz for the CORDIC and phase accumulator logic. It is realizable but expensive for this kind of FPGA speed.

Wireless and wire communication systems using digital QAM IF modulation have been limited to ASIC due to the lack of a simple algorithm to implement a high speed, low cost and low power digital QAM IF modulator. It is therefore desirable to provide a digital QAM IF modulator that can be implemented very efficiently using the basic logic structure of a FPGA, such as adders, multiplexers and ROM Look-up-tables (LUTs). The present invention provides such a device

SUMMARY OF THE INVENTION

It is an object of the present invention to provide embodiments of a digital IF modulator that can be implemented with low cost FPGAs.

It is another object of the invention is to simplify the implementation of a digital IF modulator.

Another object of the invention is to enable programmability of the digital IF modulator's carrier frequency and modulation types.

These and other objects will be apparent based on the disclosure herein.

The present invention is a digital IF modulator that can be implemented with a low cost FPGA. Only adders and LUTs are used to process highly complicated input data streams by the present simplified digital IF modulator. Only a single cycle of the IF modulated waveform is stored in the

LUT, further reducing the size of the LUT. Thus, a low speed FPGA can be used to generate a high carrier frequency output. Another aspect of this invention is the programmability of the digital IF modulator's carrier frequency and modulation types. Existing commercial wireless or wire systems such as Global System for Mobile Communications (GSM), Code Division Multiple Access (CDMA) and xDSL that use digital IF modulation of any types can benefit from this invention.

GSM, short for Global System for Mobile Communications, is one of the leading digital cellular systems. GSM uses narrowband TDMA, which allows eight simultaneous calls on the same radio frequency. GSM was first introduced in 1991. As of the end of 1997, GSM service was available in more than 100 countries and has become the de facto standard in Europe and Asia.

TDMA is short for Time Division Multiple Access, a technology for delivering digital wireless service using time-division multiplexing (TDM). TDMA works by dividing a radio frequency into time slots and then allocating slots to multiple calls. In this way, a single frequency can support multiple, simultaneous data channels. TDMA is used by the GSM digital cellular system

Code Division Multiple Access CDMA is cellular technology that competes with GSM technology for dominance in the cellular world. XDSL irefers collectively to all types of digital subscriber lines, the two main categories

being ADSL and SDSL. Two other types of xDSL technologies are High-data-rate DSL (HDSL) and Very high DSL (VDSL).

DSL technologies use sophisticated modulation schemes to pack data onto copper wires. They are sometimes referred to as last-mile technologies because they are used only for connections from a telephone switching station to a home or office, not between switching stations.

xDSL is similar to ISDN inasmuch as both operate over existing copper telephone lines (POTS) and both require the short runs to a central telephone office (usually less than 20,000 feet). However, xDSL offers much higher speeds - up to 32 Mbps for upstream traffic, and from 32 Kbps to over 1 Mbps for downstream traffic. Mbps, short for megabits per second, a measure of data transfer speed (a megabit is equal to one million bits). Network transmissions, for example, are generally measured in Mbps. When spelled MBps, it is short for megabytes per second. The term "bit" is short for binary digit, the smallest unit of information on a machine. The term was first used in 1946 by John Tukey, a leading statistician and adviser to five presidents. A single bit can hold only one of two values: 0 or 1. More meaningful information is obtained by combining consecutive bits into larger units. For example, a byte is composed of 8 consecutive bits.

It is desirable to implement FPGAs into the present Digital IF Modulator for a number of reasons. A FPGA is a low power complementary

metal oxide semiconductor (CMOS) integrated circuit that is characterized as a high performance, high speed device. It is flexible in implementation; it is programmable, re-programmable and field upgradeable. The use of these devices enables a short time-to-market because FPGAs are off-the-shelf devices in inventory. They have functional extensions and are a standard part.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A depicts a prior art digital Quadrature Amplitude Modulation (QAM) Intermediate Frequency (IF) modulator using a Numerical Control Oscillator and multipliers.

Figure 1B is a prior art block diagram illustrating how the sine IF frequency is generated by the NCO.

Figure 2 depicts a Coordinate Rotation Digital Computer (CORDIC)-based digital QAM modulator.

Figure 3 shows an embodiment of the present digital IF modulator that applies to various modulation types and offers a simple and low cost method to implement a high speed digital IF modulator using FPGA.

Figure 4A depicts the two vectors Aq and Ai with angular rotation and phase.

Figure 4B represents a 4-QAM constellation.

Figure 5 depicts a digital 64-QAM IF modulator realized using Xilinx's Virtex-II and Analog Device 10-bit D/A converter.

Figures 6A-6E depict the propagation of the digital samples **900** to **903** from **130** to **140** and finally to **200**.

Figures 7A-7C shows a converted digital to analog signal and a smoothed output.

DETAILED DESCRIPTION OF THE INVENTION

Quadrature Amplitude Modulation (QAM) provides modulation where the phase and amplitude of an input signal are changed according to message signals. These modulators are bandwidth efficient but require higher amplitude and phase accuracy. A complex input signal consists of real and imaginary parts. In digital communication, I (In-phase) and Q (Quadrature phase) are used to represent the real and imaginary parts of a complex input signal. The term is normally written as M-QAM, where M refers to the number of possible symbols. A symbol represents one point in the I/Q constellation, symbol rate is bit rate divided by log2M In a complex plane, the real part (I value) and the imaginary (Q value) of a complex number can uniquely determine its position in the plane. No phase information is needed. If the amplitude or phase noise is too high, there will not be a clean constellation, which makes it hard to detect the signal. By changing the incoming serial data streaming to a

low speed symbol, for example 64-QAM, M=64, the symbol rate is reduced log2(64)=6 times.

As discussed above, commercially available digital IF QAM modulators use sine/cosine ROMs or CORDIC and/or a number of multipliers to generate the IF modulated waveforms. Figure 3 shows an embodiment of the present digital IF modulator **850** that applies to various modulation types and offers a simple and low cost method to implement a high speed digital IF modulator using FPGA. The present architecture eliminates multipliers and sequential processing by storing the pre-computed and modulated cosine and sine carriers in ROM LUTs **800** to **803** and **820** to **823** respectively. These carriers are parallel processed in corresponding LUTs using adders **113** to **116** and registers **124** to **127**. The main processing speed of the present digital IF modulator **850** is reduced from fs to fd (fs is at least 3 times the fd for over-sampling). Fd is symbol clock rate, which is the reduced data rate after the serial to parallel block. The value of fd is based on the equation fd=fbr/k, where fbr is the input data bit stream, k = log2M and M the number of QAM constellations. LUTs, adders and registers are components of an FPGA device; they are built into the FPGA for high-speed operations involving add/sub and memory accesses cycles.

Serial-to-Parallel module **300** and I and Q Mapper **400** implement typical functions that are required by any digital modulator. The **300** module

converts input data from bit rate to symbol rate that is determined by the type of digital M-QAM modulator selected. For M=64, and fbr=96 Mbps, the fd is 16 MHz from equation fd=fbr/k, where k =log2M, fbr is the bit rate of the serial stream.

The output data of module **300** block is combined into a group of k-bits operating at a speed rate of fd fed into module **400** where I and Q are generated from a pre-selected constellation. The constellation is determined by the transmitted bit rate, available radio spectrum and the desired signal to noise ratio. The constellation selection is a compromise between radio bandwidth and acceptable bit error rate. The higher the constellation or larger the M-QAM selected, the smaller the radio bandwidth but higher the bit error rate. Once the selected constellation is determined, the I-bits and Q-bits are generated from the incoming k-bits group such that the combination of all I and Q bits will generate M-QAM constellation points. Since, it is known a priori what each constellation point waveform should be, the calculated results can be stored in LUTs and the I-bits and Q-bits can be used to generate the right point. Taking advantage of the inherent LUTs and Adders and Registers in a FPGA device, the desired waveform of each constellation point can be parallel accessed to reduced the FPGA processing speed. The Nyquist rule dictates that the digital frequency should be at least 2 times the analog frequency. For practical applications, this number is usually 4. LUTs **800** to **803** store all possible waveforms of cosine and

LUTs **820** to **823** store all possible waveform of sine. There are 4 LUTs tables for cosine and 4 LUTs for sine due to the reason explained above. Thus the output of the LUTs will generated a digitally modulated sine and cosine waveform and adders following the LUTs combine the sine and cosine into a digitally modulated QAM signal. The adders are shown in **113, 114, 115** and **116**. The registers **126** to **128** that follow the adders are provided to digitally repeat the constellation point. The multiplexers **128** to **129** are also used to output the parallel digital samples into the DAC (Digital to Analog Converter) in serial format at a final clock rate of fs=fcL, where fc is the output carrier frequency and L is the upsampling selection. Without using the present scheme, the FPGA device processing speed would have to be fs instead of fd. For high output frequency and high upsampling, the ratio fs/fd could be 10 or higher. The reduction in logic speed improves performance of the FPGA device and reduces cost.

Figure 4A depicts the two vectors Aq and Ai with the angular rotation of ωct and phase as shown.

$$In=AinCos(\omega ct+\varphi i) \qquad \text{Equation 1}$$

$$Qn=AqnSin(\omega ct+\varphi q) \qquad \text{Equation 2}$$

$$S(t)=AinCos(\omega ct)+AqnSin(\omega ct) \qquad \text{Equation 3}$$

$$Ain=AiqnCos(\varphi) \qquad \text{Equation 4}$$

$$Aqn=AiqnSin(\varphi) \qquad \text{Equation 5}$$

Where, n = 1 to M, M being the number of constellation points.

Ain and Aqn are know constellation points a priori, see Figure 4B, which depicts the 4-QAM square constellation as an example. Thus the terms Ain Cos (ωct) and AqnSin(ωct) of $S(t) = AinCos(wct) + AqnSin(wct)$.

Equation 3 can be pre-computed and stored in the ROM LUTs.

Equation 5 is a generic M-QAM IF modulator with the carrier frequency fc, and the amplitudes of Ain and Aqn. This invention eliminates all the multipliers in equations 3 through 5.

The following derivation shows how the elimination of the multipliers and the parallel processing of Equation 3 is possible. Digitally, Cos(ωct) and Sin (ωct) can be represented as

$$\text{Cos(t)}=\sum_{K=-\infty}^{+\infty} C(kT)\delta(t-KT), \qquad \text{Equation 6}$$

$$\text{Sine(t)}=\sum_{K=-\infty}^{+\infty} Si(kT)\delta(t-KT), \qquad \text{Equation 7}$$

where T is the period of the delta function, Cos(t) is the discrete representation of Cosine in time domain, C(KT) is the amplitude of the Cosine at K sample of period T, Sine(t) is the discrete representation of Sine in time domain and Si(kT) is the amplitude of k sampled at T period.

Figure 4B represents the 4-QAM constellation. Clearly, the Ain and Aiq are the magnitudes of the constellation's points. These magnitudes are scaled appropriately depending on the information pair (I,Q) and another word. If I and Q represent indexes of the two dimension array, then the exact constellation's position can be retrieved without performing multiplications as shown in equation 5 and 6.

Equation 4 shown in digital representation is:

$S(t)=Ain\ (\Sigma C(kT)\delta(t-KT))+Aqn\ \Sigma Si(kT)\delta(t-KT)$,

Or

$$S(t)=\left[\left(Ain\sum_{K=1}^{L}C(kT)\right)+\left(Aqn\sum_{K=1}^{L}Si(kT)\right)\right]\sum_{-\infty}^{+\infty}\delta(t-KT) \qquad \text{Equation 8}$$

Or

$$Ain\sum_{K=1}^{L}Cos(kT)=Ain[(Cos(T)+Cos(2T)+Cos(3T)+...Cos(LT)]$$

$$=Ain(Cos(T)+Ain\ Cos(2T)+AinCos(3T)+...AinCos(LT)$$

$$Aqn\sum_{K=1}^{L}Si(kT)=AqnSi(T)+AqnSi(2T)+AqnSi(3T)+...AqnSi(LT)$$

$$S(1)=AinC(T)+AqnSi(T) \qquad \text{Equation 9}$$

$$S(2)=AinC(2t)+AqnSi(2T) \qquad \text{Equation 10}$$

$$S(3)=AinC(3T)+AqnSi(3T) \qquad \text{Equation 11}$$

$$S(4) = AinC(4t) + AqnSi(4T) \qquad \text{Equation 12}$$

$$S(L)=AinC(Lt)+AqnSi(LT) \qquad \text{Equation 13}$$

Where, S(1) ... S(L) are discrete sums of IF modulated cosine and sine.

Ain and Aqn are known magnitudes from the QAM modulation constellation selected a priori. C(T) .... C(LT), Si(T) ... Si(LT) are amplitudes of the cosine and sine waves scaled by the appropriate symbol data Ain and Aqn. The single cycles of pre-computed values of Ain, Aqn, and the cosine and sine samples can be stored in the ROMs, thus eliminating the need for multiplications. Only adder circuits are required for generating the digital IF modulated carrier. The numbers of adders corresponds to the up-sampling L. The other important aspect of this invention is the parallel processing of the S(1) to S(L). Since the Ain and Aiq are changing at the symbol rate, which is much slower than the sampling rate, δ(t-KT), low power and cost can be achieved with FPGA or ASIC devices. If the S(t) were implemented sequentially as in the prior art, multiplication and addition circuitry would have to operate at the sampling rate, δ(t-KT).

The invention is demonstrated via an implementation of digital IF modulator for 64-QAM. Figure 5 depicts a digital 64-QAM IF modulator realized using Xilinx's Virtex-II and Analog Device 10-bit D/A converter. The 64-QAM IF modulator generates a carrier frequency of 80 MHz with the bit rate 96 Mbps.

Figure 5 shows the FGPA implementation of **300, 400** and **850**. Analog device 10-bit D/A is interfaced to the FPGA via ribbon cable connection.

Serial-to-Parallel module **300** and I and Q Mapper **400** implement typical functions that are required by any digital modulator. The **300** module converts input data from bit rate to symbol rate that is determined by the type of digital M-QAM modulator selected. For M=64, and fbr=96 Mbps, the fd is 16 MHz from:

$$fd = fbr / k \qquad \text{Equation 14;}$$

$$fs = fcL \qquad \text{Equation 15; and}$$

$$fmux = fs / 2 \qquad \text{Equation 16.}$$

The output of module **300** block is fed into module **400** where I and Q are generated as selected constellations. The output of **400** are 3-bit I and 3-bit Q data toggled at the 16 MHz clock rate. Each of the 3-bit I and Q data are fed directly to the **800** to **803** and **820** to **823** as shown. The content **800** stores the first sample of all modulated cosine waveform scaled appropriately by Ain and Aqn data. Similarly, **801** to **803** are for samples 2 to 4. I/Q simultaneously address the contents of **800** to **803** and **820** to **824**. The result of the **800** to **803** is added to the **820** to **823** respectively using adders **113** to **116**. The adders' outputs are latched by registers **124** to **127** to maintain the modulated carrier waveforms for fd's duration. The sampled outputs are multiplexed via MUX modules **128** and **129**, which reduce the speed of the sample output to fs/2. Module **128** transfers the

1st and 3rd samples and module **129** transfers the 2nd and 4th samples of each IF modulated waveforms. Figures 6A-6E depict the propagation of the digital samples **900** to **903** from **130** to **140** and finally to **200**. As seen from Figures 6A-6E, the digital samples **900** to **903** are sums of the samples pairs **(700, 704)**, **(701, 705)**, **(702, 706)** and **(703, 707)** from Figure 5. Each of those samples are parallel processed and interleaved in modules **128** and **129** and sequentially processed in the D/A at 320 MHz. An off-the-shell D/A device and LPF are used to convert the digital to analog signal and to smooth the output (Figures 7A-7C).

The foregoing description of the invention has been presented for purposes of illustration and description and is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. The embodiments disclosed were meant only to explain the principles of the invention and its practical application to thereby enable others skilled in the art to best use the invention in various embodiments and with various modifications suited to the particular use contemplated. The scope of the invention is to be defined by the following claims.